ABSTRACT OF THE DISCLOSURE

Described are methods for accurately measuring the skew of clock distribution networks on programmable logic devices. Clock distribution networks are modeled using a sequence of oscillators formed on the device using configurable logic. Each oscillator includes a portion of the network, and consequently oscillates at a frequency that depends on the signal propagation delay associated with the included portion of the network. The various oscillator configurations are modeled mathematically as the sum of a series of delays, with the period of each oscillator representing the sum. The respective equations of the oscillators are combined to solve for the delay contribution of the included portion of the clock network. The delay associated with the included portion of the clock network can be combined with similar measurements for other portions of the clock network to more completely describe the network.